Demonstrator of Three Prototypes of Read/Stim Units

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Project Acronym: B-CRATOS

Project Title: Wireless Brain-Connect inteRfAce TO machineS

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Approvals

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Executive Summary

This report details the progress on D2.4, a demonstrator of read and stimulation prototypes. The aim of this report is to provide the latest developments and test results for system integration. The integration plans involve assembling all the BRME ASIC chips and circuits with the NTNU backscatter high data rate communication module and providing stimulation commands and telemetry readout for the provisional implant module in three steps: 1) Integration Development Model (IDM-1), where the demonstrator uses distributed modules and signal emulators for proof of principle; 2) IDM-2, where the system will be assembled and integrated on a modular platform with interconnectivity between BRME and NTNU circuits; 3) IDM-3, an operational assembled system with neural recording and data connectivity to be used with NHP testing and demonstration.

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Table of Contents

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 965044

1 Overview

1.1 Purpose

This public report delineates how the Work Package 2 (WP2) system design aligns with the B-CRATOS product and subsystem requirements. The primary aim of WP2 is to establish a brain implant system, along with its accompanying external tools and devices, capable of fully wireless operation. This is to be achieved through the development and integration of technologies enabling high data rate wireless neural reading, command and control for stimulation and telemetry, as well as wireless power transfer to sustain implant operations. The implant technology and its external support system under WP2 will facilitate bidirectional communication with neurons and exchange communication data with the FAT-IBC module, enabling connectivity to the robotic arm.

1.2 B-CRATOS Partners

Short Name	**Full Name**
UU	Uppsala Universitet
SINANO	Institut Sinano Association
SSSA	Scuola Superiore di Studi Universitari e di Perfezionamento S'Anna
BRME	Blackrock Microsystems Europe GmbH
LINKS	Fondazione LINKS – Leading Innovation & Knowledge for Society
DPZ	Deutsches Primatenzentrum GmbH
NTNU	Norges Teknisk-Naturvitenskapelige Universitet NTNU

1.3 Responsibilities

NTNU leads deliverable D2.4 within the B-CRATOS project, assuming responsibility for integrating the BRME neural interface ASIC chip with NTNU's wireless communication modules. This integration aims to establish connectivity between the ASIC and the implant electronic system, further linking this unit with the wearable reader and powering electronics. Prof. Ali Khaleghi, from NTNU, serves as the WP2 project leader, bearing scientific and technical responsibilities. Dr. Aminolah Hasanvand, NTNU technical researcher, provides support for the implant electronics and integration. BRME collaborates closely with NTNU, focusing on integrating the developed ASIC with wireless technologies into the implantable neural interface device to fulfill WP2 tasks, deliverables, and milestones. Prof. Robin

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Augustine, from UU, acts as the scientific coordinator, assuming overall project, scientific, and technical responsibility. In his role as B-CRATOS coordinator, Prof. Augustine reviews, approves, and submits deliverables and reports.

1.4 Definitions

Term	**Description**
ASIC	Application-specific integrated circuit, a chip customized for a particular function
AI	Artificial intelligence
B-CRATOS	the Wireless Brain-Connect inteRfAce TO machineS project
BCI	Brain-Computer Interface
Fat-IBC	Fat intra-body communication
M1	Primary motor cortex, the region of the brain involved in the planning and execution of voluntary movement
SPI	Serial Peripheral Interface
NHP	Non-human primate
stimulation, stim	Direct electrical brain stimulation
UEA	Utah electrode array
WPT	Wireless power transfer
IDM	Integrated Development Model

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2 Brief Description of WP2 Tasks and achievements

We aim to provide an implant neural wireless interface that integrates: 1) Utah electrode array (UEA); 2) BRME channelling amplifier and stimulation ASIC; 3) NTNU interface with BRME ASIC for 16/32 Mbps neural data streaming; 4) NTNU two-way telemetry and stimulation command interface 5) Wireless powering of the implant unit. The implant is supported by a wearable external system that interfaces with the integrated implant unit to carry the neural read/stim data via FAT-IBC (WP3) to the prosthetic arm AI system. Figure 1 shows the connectivity modules.

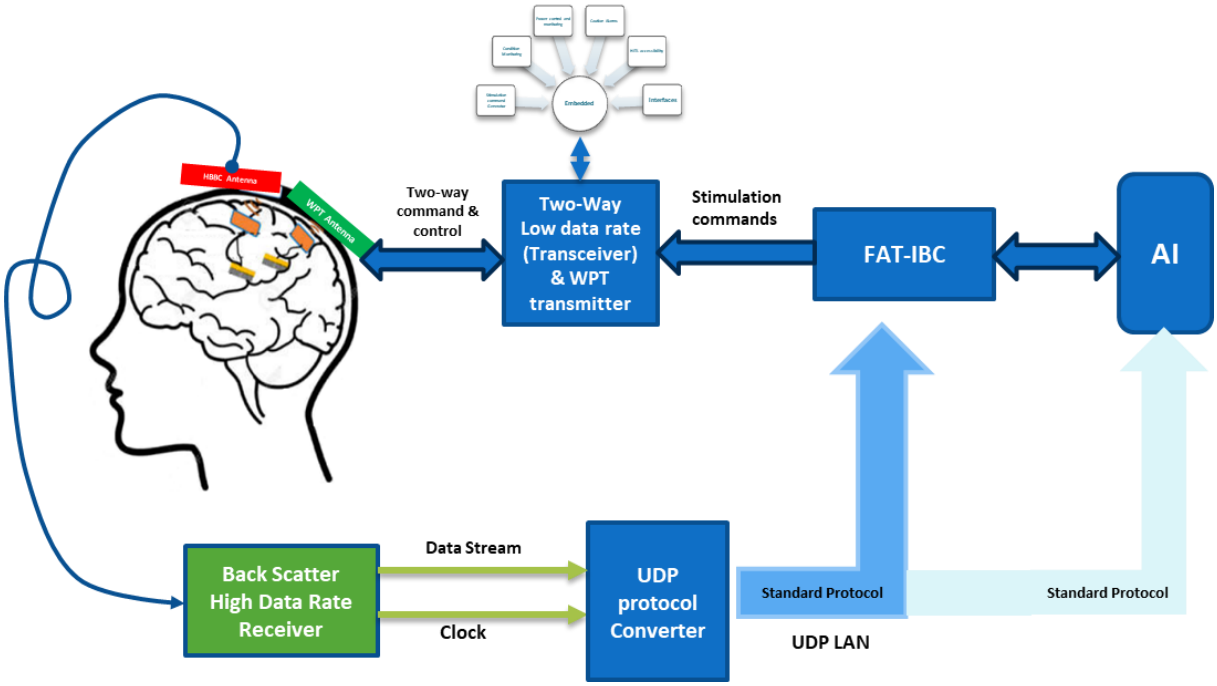

Figure 1. **Two way connectivity block diagram from the implant to prosthetic AI module**

The Integrated Development Model (IDM-1) has been reported as part of MS3 and MS4. In these milestones, we have demonstrated a bench setup operation of FPGA emulated readout data, directed to the backscatter electronics that simulates a data rate of 16 Mbps and 32 Mbps, which is communicated to the backscatter remote reader at a distance of 1-2 cm—the potential spacing between the under-skin implant and the wearable reader antenna. In this model, we have optimized our reader system software to decode the streamed data and have also developed monitoring software that measures the bit error rates, assuming a known data is transmitted from the FPGA. Further development towards D2.4 includes demonstrating the functionality of the stimulation data link via magnetic coupling, where we can supply a command link of 400 Kbps to the implant emulator board and confirm data reception in the IDM-1 model. In this regard, the necessary external software to interact with the data handled from the AI module and translate this information to the implant microcontroller system has

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been verified. The principal operation of the system, including backscatter and magnetic coupling, has been validated in an animal study using a pig model under general anaesthesia.

2.1 Integrated development model-2 (IDM-2)

The IDM-2 serves as an intermediate step towards the final demonstrator, IDM-3, in the NHP animal study. This phase replaces the FPGA emulator (IDM-1 in the bench-top model) with the BRME ASIC device. The first version of the BRME V1 ASIC was delivered in October 2023, followed by an updated V2 in April 2024. In the current integration stage, we are incorporating the BRME ASIC with the NTNU modules as illustrated in Figure 2. This model advances towards a realistic lab model where the ASIC's performance has been validated for acquiring neural information via Utah array neural emulators.

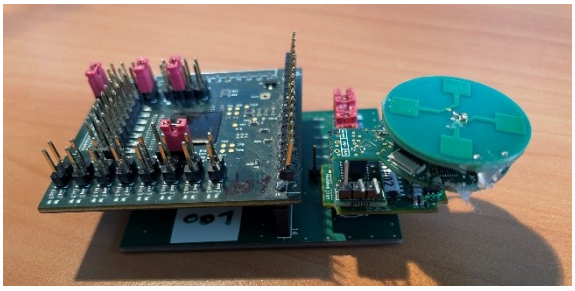

Figure 2. **ASIC V1 integrated with the NTNU implant module (IDM-2)**

The system connects to a neural spike emulator generator that can supply specific or emulated waveforms to the ASIC module. The signal level matches real neural signals, and the ASIC's amplifier and channels, together with digitalizers, stream the recordings to a single output data line. The data then feeds into the NTNU backscatter unit, which controls the backscatter antenna load impedance with minimal power. This setup ensures continuous data streaming with less than 10 msec latency, directly accessible to an external reader. Furthermore, the ASIC receives commands via the SPI bus from the NTNU microcontroller unit to generate stimulation waveforms required for feedback control of neurons. IDM-2's PCB integration with test modules reduces the connectivity of communication lines, aiming to minimize the interference observed with IDM-1. The IDM-2 operates on an external power supply, which ensures stable operation for readout and stimulation voltage level generation, thus enhancing system programming and stability in lab models.

With the introduction of ASIC V1, we began developing the interface between the microcontroller unit and the ASIC, which involves significant hardware and software developments. This process requires precise timing, command exchange, and data connectivity. As the system's data rate is significant, multiple factors influence communication quality; thus, signal integrity and hardware design are rigorously tested in subsystems and individually. Figure 3 depicts the ASIC V2 and its provisional integration with the NTNU implant unit. Given the compact and modular platform of the interconnection lines, further measurements and updates to the NTNU hardware and software are necessary to align with

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these new developments. This constitutes an ongoing collaborative research and development effort with NTNU and BRME partners. The subsequent phase, IDM-3, will focus on packaging the system into a test setup compatible with NHP studies.

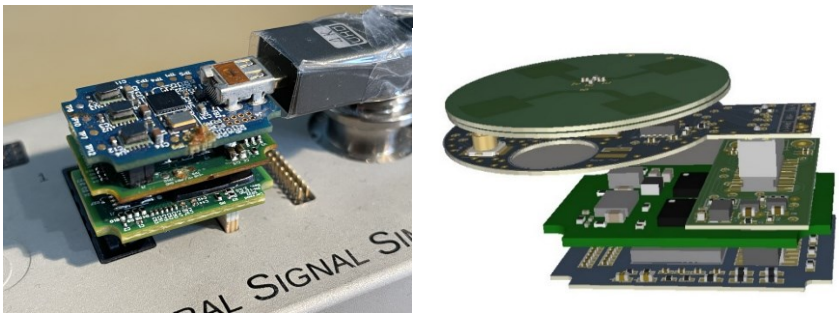

Figure 3. **BRME ASIC V2, modular integration with NTNU system (IDM-3)**

To successfully complete and deliver the final integrated module for IDM-3, our efforts are divided into two distinct sections, as illustrated in Figure 4. The first section, the implant unit integration, concentrates on maintaining signal integrity. This involves precise engineering to ensure reliable signal transmission within the implant itself. The second section focuses on the external interface, which connects with the implant to facilitate high data rate reading and robust connectivity. This includes integrating all standard interfaces and interconnections with subsequent systems such as the FAT-IBC and AI. Additionally, it manages the stimulation data transfer to the ASIC, including signal generation and verification. For IDM-2, our emphasis has been on enhancing the interconnectivity between the local implant and wearable devices, using standard communication protocols to ensure compatibility and ease of integration.

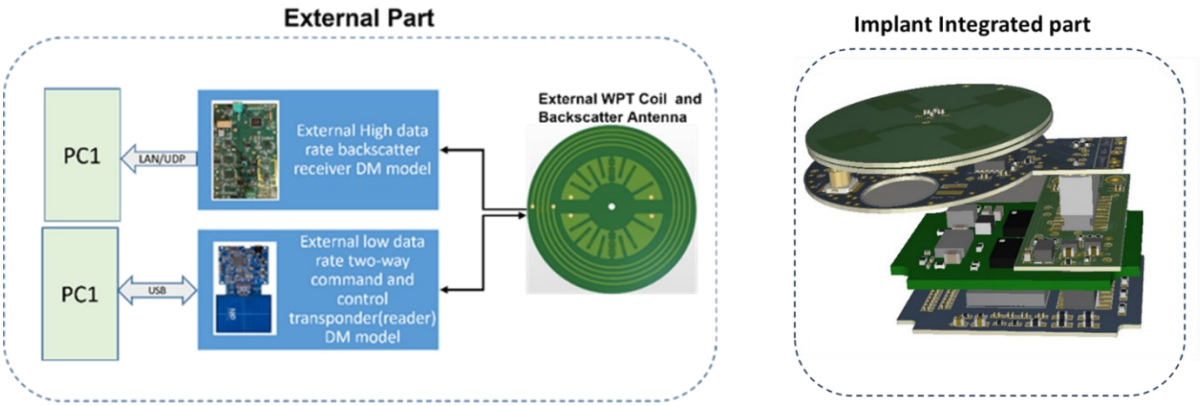

Figure 4. **IDM-2 Implant Integrated Module Including Electronics, Antennas and RF Systems, and External Module Including RF Reader System, Backscatter Data Interface, and Stimulation Command and Telemetry Links.**

2.2 Progress Overview of the IDM-3

The IDM-3 represents a pivotal advancement in neural interface technology, aimed at enhancing connectivity and data transfer capabilities in neuroprosthetic devices. As we progress towards the final demonstration phase, significant strides have been made in the

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development and integration of key components. Parts of these activities are ongoing and require significant test and verification and we assume to collaboratively complete these for NHP test.

2.2.1 Antenna and Connectivity Enhancements

A newly designed tunable backscatter reader with an external antenna marks a significant improvement in minimizing interference and maximizing data transmission efficiency. This design supports high data rate operations with minimal Bit Error Rate (BER), crucial for reliable neural data acquisition. The finalized CAD model of the antenna has been integrated with the implant system and is poised for fabrication, ensuring optimized performance for forthcoming field tests.

2.2.2 Hardware and Software Integration

The implant main board has been revised to incorporate state-of-the-art components such as NXP-NFC for wireless power and bidirectional communication. These modifications are designed to enhance the interface with the ARM microcontroller and BRME ASIC V2 device, improving overall system reliability and signal integrity. Concurrently, software developments have been underway to support high-rate neural transmission and efficient power management. The software is tailored to seamlessly integrate with the new hardware configurations, facilitating robust communication and data management capabilities.

2.2.3 Reader System and Interface Upgrades

Our external reader system continues to support robust RF communication with the implant. Modifications to support higher data rates are planned, which will allow us to meet the increasing demands for faster and more reliable data transmission. In parallel, the external reader interface has been successfully converted to support standard UDP protocol, making it compatible with modern network systems and enhancing its readiness for integration into broader communication networks.

2.2.4 Commitment to Electromagnetic Compatibility

In the IDM-2 and IDM-3 developments, ensuring electromagnetic compatibility (EMC) is of paramount importance, particularly as the integration of the current ASIC and RF systems must operate flawlessly in high-field environments. Initial tests with the IDM-1 microcontroller system showed minimal electromagnetic interference, setting a robust foundation for further evaluations. We are now conducting detailed assessments of the RF reader's impact on ASIC functionality and the overall operation of the IDM-2, along with tests on NFC capabilities and their interaction with RF systems during both operational and power modes within the implant.

2.2.5 Preparing for In-Field Trials

As we prepare for in-field trials, particularly in NHP studies, the importance of rigorous field testing becomes even more critical. The RF and NFC systems may potentially introduce significant disruptive signals to the neural transmission lines between the Utah array and the

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implant module. To address this, planned evaluations at the DPZ facility are focused on meticulously observing the effects of RF and NFC on neural signal integrity using the animal implant unit. These trials are designed to thoroughly assess the RF system's performance in various scenarios, as elaborated in the electromagnetic compatibility document of WP2. This careful testing ensures that our systems can effectively manage and mitigate any potential interference, maintaining the integrity and reliability of neural data transmission in practical, real-world applications.

2.3 Advanced Developments in ASIC V2 Interface and Integration

2.3.1 Enhancements in Neural Signal Acquisition and Stimulation

BRME has achieved a significant milestone in neural technology by designing, constructing, and successfully testing six ASIC Interface Boards featuring the innovative Stim/Record ASIC. These boards are crucial for high-data-rate neural signal acquisition and direct current stimulation, supporting up to 32 channels. The modular nature of these boards facilitates rapid prototype modifications, which is vital for adaptive testing and development.

The boards include an Omnetics connector, which is compatible with the standard Blackrock headstage, paving the way for future in vivo demonstrators. Verification tests conducted by BRME have confirmed the boards' functionality in configuration, data read-out, SPI/digital command processing, and stimulation, enhancing the overall performance verification of the ASIC, carried out in collaboration with international partner Blackrock Neurotech.

To further support sophisticated neural data readout and stimulation, both at the bench and in live environments, BRME has developed ASIC-compatible wired interface boards. These boards utilize an FPGA and a standard micro HDMI I/O interface, enabling seamless integration with external neural recording hardware and software.

2.3.2 Visual Demonstrations of Performance

Figure 5 displays the Stim/Record ASIC in a test setup connected via a wired HDMI adapter, situated on a Neural Signal Simulator device. Figure 6 illustrates the readout verification of the Stim/Record ASIC over a wired adapter connection. The middle traces in blue and green represent input signals, the top trace in yellow shows the multiplexed output from the ASIC, and the bottom trace in pink depicts the recovered digital output signal from a single channel. Figure 7 demonstrates the stimulation pulse train verification, showing a pulse train (50 microamps) controlled via a wired digital controller.

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Figure 5. **Stim/Record ASIC in test configuration with wired HDMI adapter. Placed on Neural Signal Simulator device.**

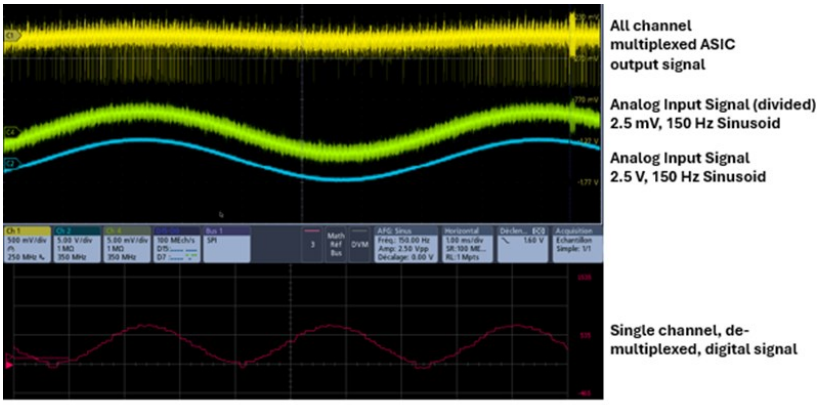

Figure 6. **Stim/Record ASIC readout verification over wired adapter connection. Middle, blue and green traces: input signals; Top, yellow trace: multiplexed output from ASIC; Bottom, pink trace: single channel recovered digital output signal.**

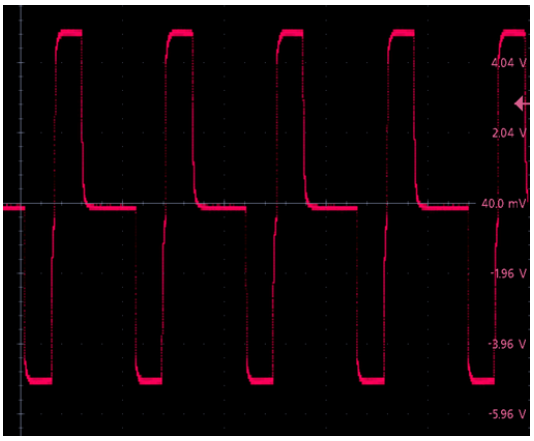

Figure 7. **Stim/Record ASIC stimulation pulse train verification, demonstrating a pulse train (50 microamps) via wired digital controller.**

2.3.3 Integration of Prototype Devices

BRME has also demonstrated the physical integration of the ASIC Interface Board with NTNU's wireless implant electronics and antennas, a critical step toward the practical application of these technologies in medical devices. With materials on hand to construct at least three prototype devices for further testing, and additional units planned for future studies, this collaboration underscores our commitment to advancing neural interface technology Figure

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8 shows the physically integrated system in a modular structure designed to facilitate IDM-2 testing.

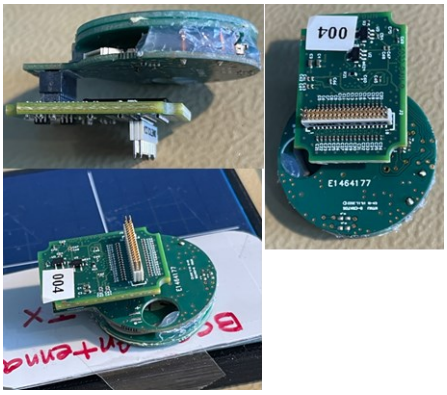

Figure 8. **Physical integrated system in modular structure to support IDM-2 test.**

3 Conclusion

This public report outlines progress toward deliverable D2.4, targeting test prototypes for NHP experiments. The setup is divided into three IDMs. IDM-1 is related to a benchtop setup with an FPGA emulator and testing of backscatter at 16, 32 Mbps, and NFC communication at 400 kbps, as well as wireless powering up to 40 mW. IDM-2 integrates the BRME ASIC V1 chipset for system integration, programming, and interface with the NTNU wireless and powering unit. The system integration in IDM-2 has helped the team to interrogate between the developed systems and significant advancements have been made, which are also underway to accomplish. IDM-3 integrates the ASIC V2 with a focus on EMC and system interference, and new PCB developments for animal studies from an NHP use perspective. Development in IDM-3 is underway.

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